

Companies Collaborate to Streamline MMIC Design and Development

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High-performance applications such as fiber optic networks, third-generation (3G) wireless and millimeterwave radios are driving the demand for monolithic microwave integrated circuits (MMICs). To keep ahead of the competition, companies need to get chips designed and fabricated more rapidly and with a higher certainty of success.

A new three-party initiative from Applied Wave Research (AWR), TriQuint Semiconductor (TriQuint) and Multilink Technology Corporation (Multilink), called Fast Chips, is designed to streamline all aspects of gallium arsenide (GaAs) MMIC development. The process provides new levels of automation to MMIC and radio frequency integrated circuit (RFIC) to designers by developing foundry libraries and methodologies that accelerate the introduction of complex MMIC products.

This article presents a four-stage distributed amplifier (DA) and transimpedance amplifier designs for fiber optic applications including measured versus modeled data.

Introduction

Effectively designing MMICs has been challenging and time-consuming ever since the first GaAs foundries opened to the public in the 1980s. Unfortunately for designers, the development methodology has remained difficult in spite of the numerous advances in both process technology and electronic design automation (EDA) tools. One of the limiting factors has been a disconnection between customers, foundries and EDA suppliers.

Fast Chips is an industry initiative that brings together industry leaders to work on design flow issues and deliver commercially

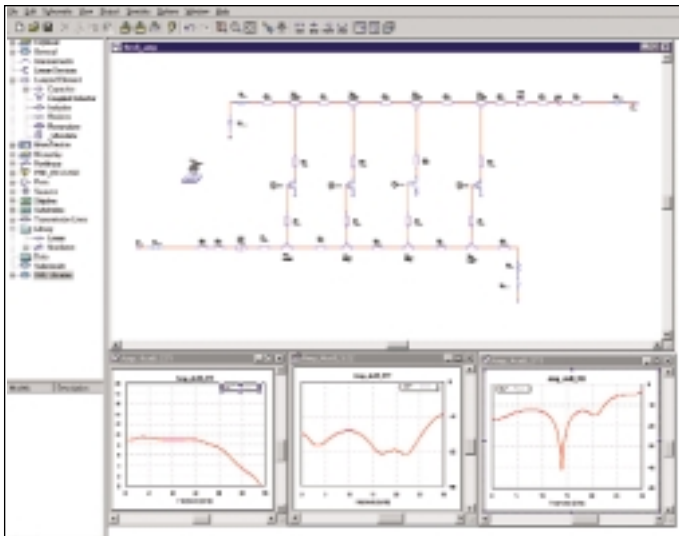
available process design kits (PDKs) that streamline the development and manufacturing sign-off process for MMICs. Multilink, a provider of advanced semiconductor-based solutions designed to accelerate the deployment of high-speed optical networks, has been the primary driver of the Fast Chips initiative.

Multilink realized its existing EDA tools and design flow required improvements to maintain fast design cycles. The company's microwave IC development process was unable to keep up with the demands of the rapidly progressing communication industry, so it turned to AWR and TriQuint to close the product development gap. This collaborative approach has enabled Multilink to significantly streamline its design flow and, as an added benefit to customers, improve time-to-market. The Fast Chips initiative has not only reduced design time but also increased the performance and quality of Multilink's microwave designs.

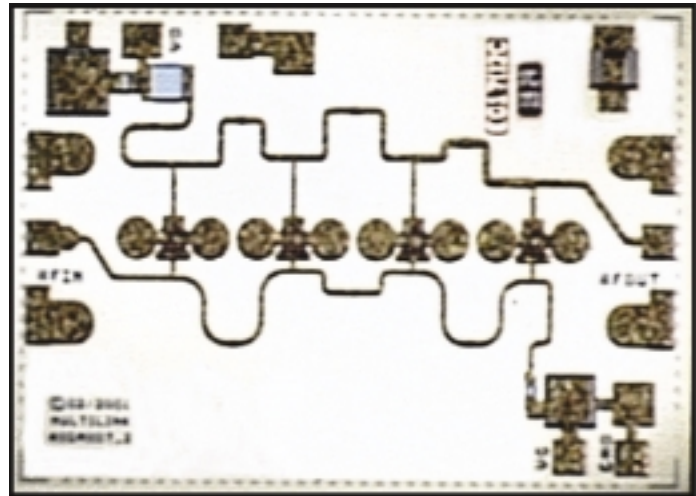
What is Fast Chips?

The Fast Chips initiative was started to develop commercially available technology to expedite the development of GaAs ICs. AWR developed the Microwave Office 2002 design suite to address the requirements of advanced MMIC design, but to fully use this modern EDA platform, close cooperation is required from foundry partners and end-users.

"Working in collaboration with Triquint and Multilink enabled us to step back and rethink what a foundry PDK could be," said David Neilson, director of the MMIC market segment at AWR. "Once we began to focus on the chip life-cycle as a whole, instead of just incremental changes to the current way of doing things, the



▲ Figure 1. Multilink four-stage distributed amplifier and corresponding simulations in AWR's Microwave Office 2002 Design Suite.



▲ Figure 2. Multilink four-stage distributed amplifier.

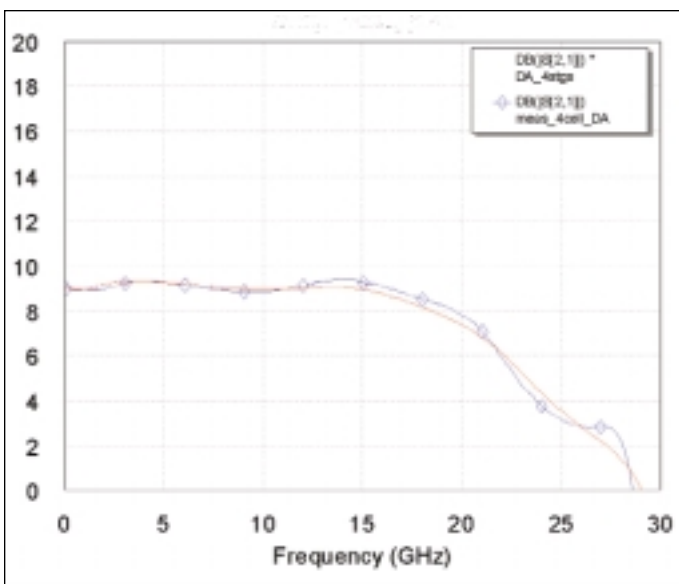
Four-stage distributed amplifier

The schematic diagram shown in Figure 1 is a four-stage DA circuit developed by Multilink. This broadband design, developed using the Fast Chips methodology, is based on TriQuint's 0.25 μm pseudomorphic high-electron mobility transistor (pHEMT) process. The design goals were 9.5 dB gain from direct current (DC) to 20 GHz with better than 12 dB of return loss and an ability to operate with greater than 10 dBm total output power. The chip uses a 3-volt supply and dissipates 120 milliwatts. The final layout, depicted in Figure 2, was completed in significantly less time and with closer correlations between measurement and simulations compared to previous design efforts.

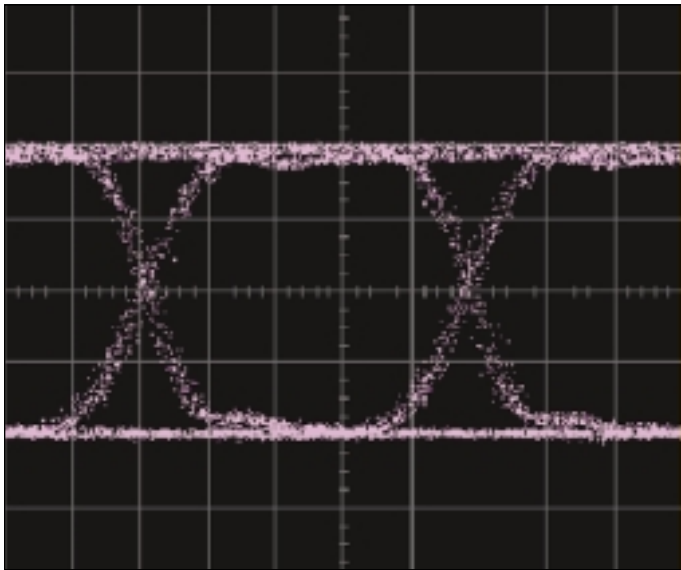
Figure 3 shows the frequency domain performance which indicates the correlation of measured versus simulated gain from DC to greater than 25 GHz. Even with close correlation in the frequency domain, an additional test of fiber optic circuits is the performance in the time domain. Figure 4 shows the measured time domain performance of the four-stage DA measured at a data rate of 10.7 gigabits per second (Gb/s). Time domain measurement capabilities are an increasingly important capability in microwave EDA solutions for fiber optic requirements. With direction from Multilink, AWR added capabilities including modulated signal analysis and EYE diagrams to support the analysis of fiber optic circuits using harmonic balance simulations.

New high-density process technologies

TriQuint, in parallel with EDA advancements, has developed a high-density interconnect (HDI) process to reduce the cost of commercial MMICs by facilitating denser layouts that can reduce chip area and increase yields. The HDI process is the first commercially available pHEMT process that supports three levels of interconnect metalization.



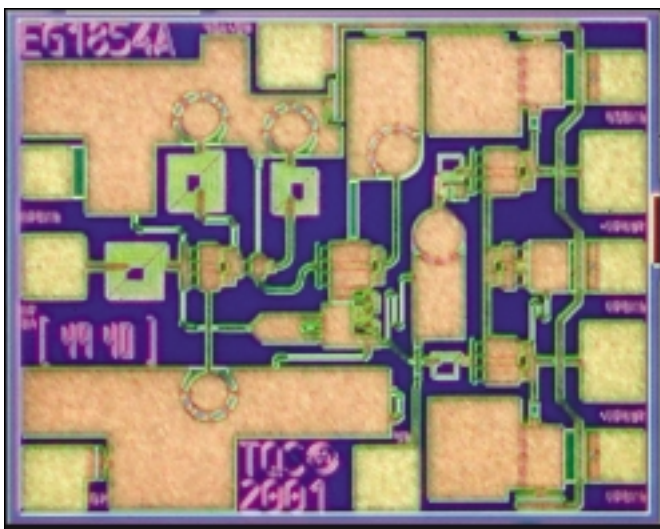
▲ Figure 3. Simulated versus measure gain for the four-stage DA.



▲ Figure 4. Measured EYE diagram of the four-stage DA at 10.7 Gb/s with a 231-1 bit pattern.

“We developed the HDI process to facilitate lower-cost, higher-performance circuits,” said Lisa Howard, foundry services manager at TriQuint. “However, external customers could not take full advantage of this process technology because existing EDA tools were not capable of supporting the layout issues efficiently. Fast Chips is facilitating the use of advanced processes, such as HDI, by developing robust parameterized cell libraries that enable users to take full advantage of the foundry process.”

The underlying technology in the Microwave Office 2002 software is more easily customized to support an advanced MMIC process such as HDI. The MMIC design process is different from the traditional “digital” EDA design flow in that it is a very interactive process where the designer must oversee and verify every aspect of the



▲ Figure 5. TriQuint TGA4805 transimpedance amplifier.

design, including its physical representation. As the design moves through its design cycle, the MMIC designer is burdened with synchronizing all the representations of the circuit. Any inconsistency between representations or missed detail will inevitably have a profound effect on the electrical performance.

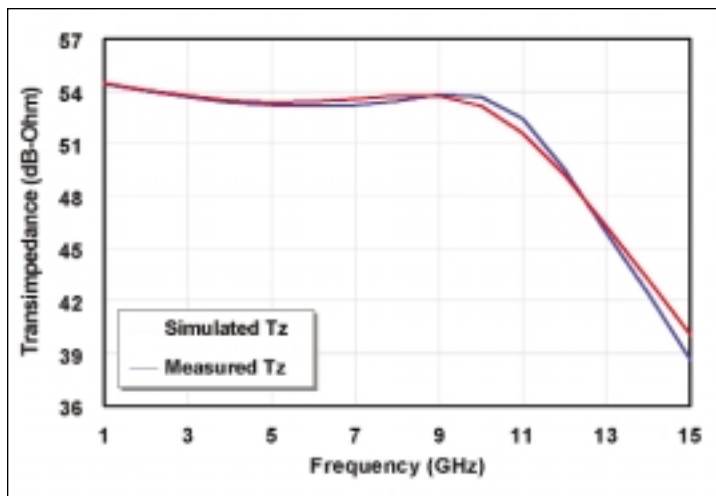
The Microwave Office 2002 design suite uses advanced computer science algorithms to eliminate problematic “design synchronization” or “back annotation” routines. This approach enables MMIC designers to work from the layout with direct access to simulation results. By maintaining a single object-oriented database for schematic entry, layout and simulation, designers get virtually instantaneous feedback on the changes they make to a design.

Electromagnetic (EM) analysis, DRC and three-dimensional (3D) views are also important capabilities required to support advanced semiconductor technologies, such as HDI. In addition, the integrated 3D views provided by the software are especially well-suited for visualizing and correcting interconnect issues that can arise with complex, state-of-the-art microwave process technologies, such as TriQuint pHEMT HDI.

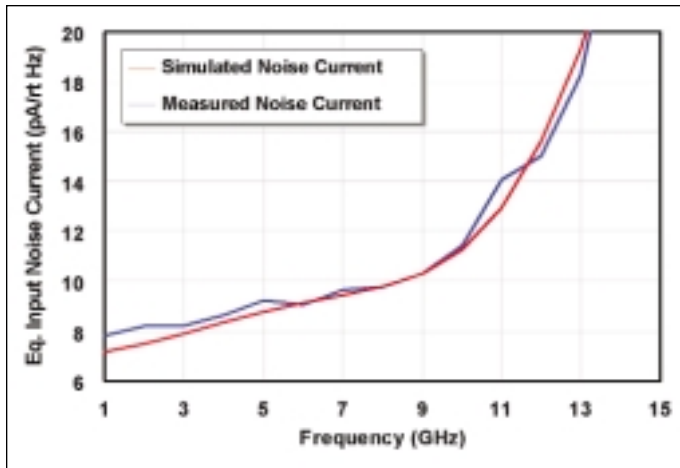
A 10 GB/s differential transimpedance amplifier (TIA)

Fiber optic MMICs must operate over extremely broad bandwidths, typically from near DC to beyond 20 GHz. OC-192/STM-64-based products operate at 10 Gb/s and typically must operate beyond 10 GHz, and next-generation OC-768 products will operate at 40 Gb/s.

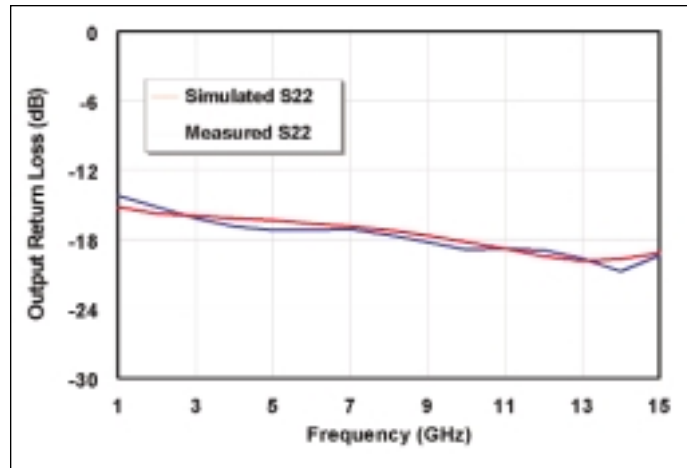
The TriQuint TGA4805-EPU, shown in Figure 5, is a wideband TIA with differential outputs that provides 500-ohm single-ended transimpedance into a 50-ohm termination (1,000-ohm differential into a 100-ohm termination). Simulations of the MMIC were carried out using Microwave Office 2002 software and compared to measured data. Figure 6 shows measured versus simulated transimpedance as a function of frequency.



▲ Figure 6. TGA4805 simulation versus measured transimpedance versus frequency.



▲ Figure 7. TGA4805 simulation versus measured equivalent input noise current.



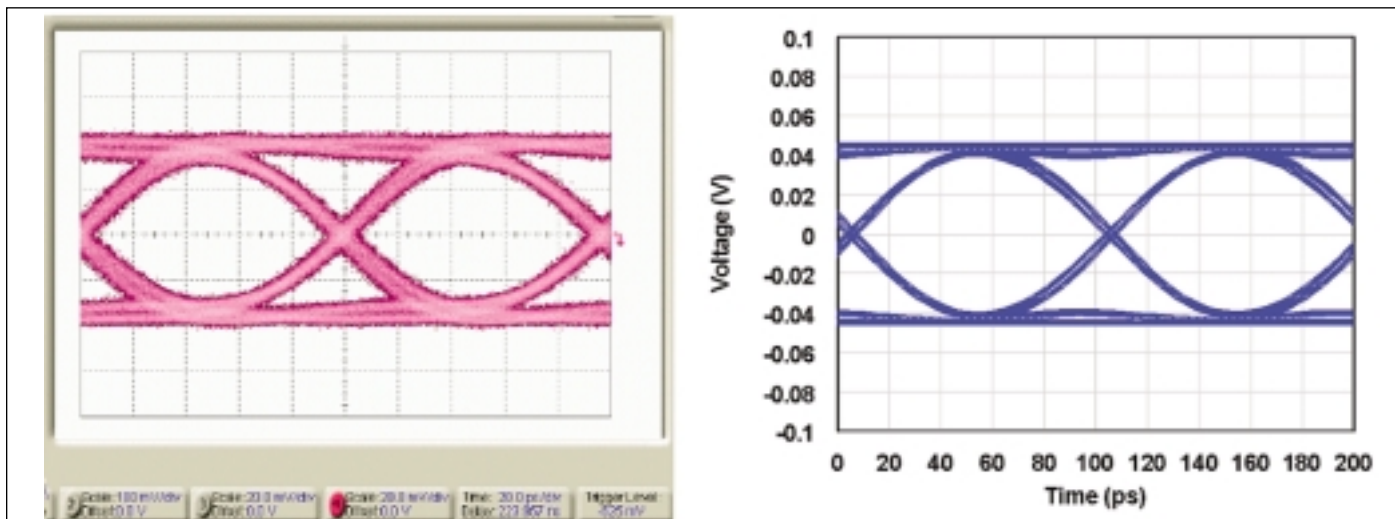
▲ Figure 8. TGA4805 simulation versus measured output return loss.

The chip, which operates from a single +5-volt supply, typically dissipates 225 milliwatts of DC power. The TGA4805 die size is 1.1×0.91 mm and has DC-coupled RF ports. The device is backside grounded with vias and requires no grounding bond wires. Typical output return loss is greater than 15 dB; measurement versus simulation data shown in Figure 7. The average equivalent input noise current, displayed with measurement versus simulation (see Figure 8), is $9 \text{ pA}/\sqrt{\text{Hz}}$ at 1 to 10 GHz. Typical 3 dB BW is 30 kHz to 11 GHz, with 0.2 pF of photodiode capacitance.

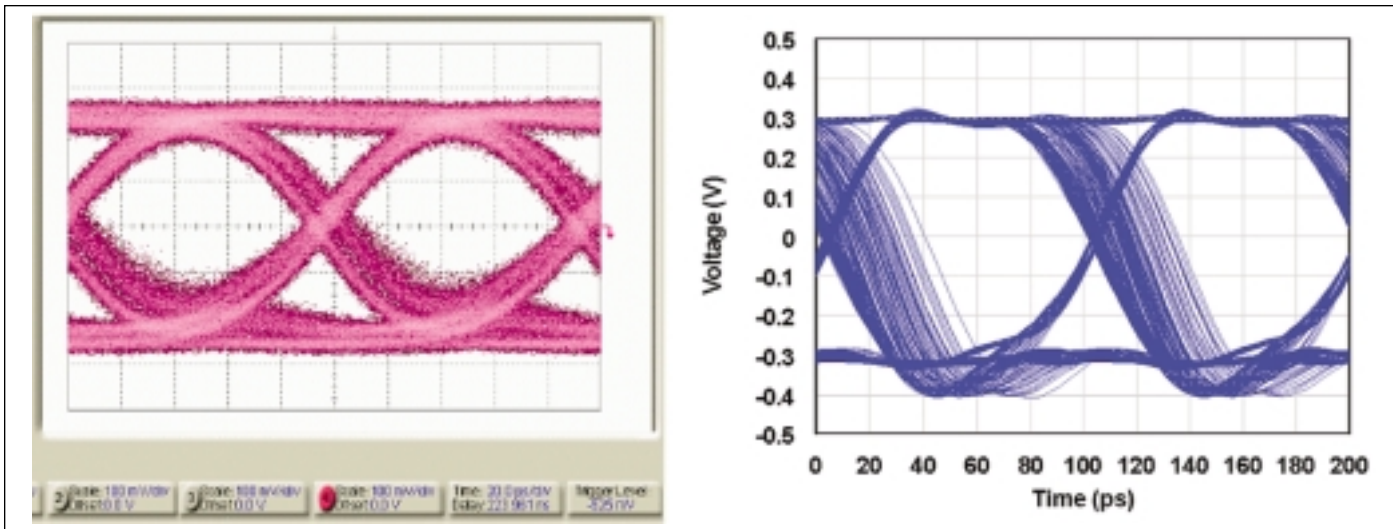
Although the relative performance of these circuits can be measured in the frequency domain, specifications are defined with time-domain measurements such as EYE diagrams, shown in Figures 9, 10 and 11. Using modulated signal analysis with the harmonic balance technique, it is possible to measure the time domain response even at high-power levels with long bit sequences. Excellent agreement between simulation and

measurement was obtained.

The Fast Chips initiative also focused on building a PDK that could dramatically accelerate the MMIC design process specific to Triquint. The library was built with fundamental circuit building blocks that included schematic representations, Triquint's proprietary electrical models and correct-by-construction parameterized layout cells. Then "bridge" code was added that creates intelligent interconnects between transmission lines and cells. For instance, HDI has 10 different line types composed of different plating combinations of the three independent metal layers. When the designer changes line types or connects a line of a given type to a cell, the bridge code automatically creates the correct connection. This may include extending the nitride layers or even building interlayer contacts with vias. In any case, the microwave designer no longer needs to be an expert in regards to the numerous geometry rules necessary for processing. Add to that a DRC library that includes a



▲ Figure 9. TGA4805 simulation versus measured data EYE diagram for optical input power at a linear condition.



▲ Figure 10. TGA4805 simulation versus measured data EYE diagram for optical input power approaching overload condition.

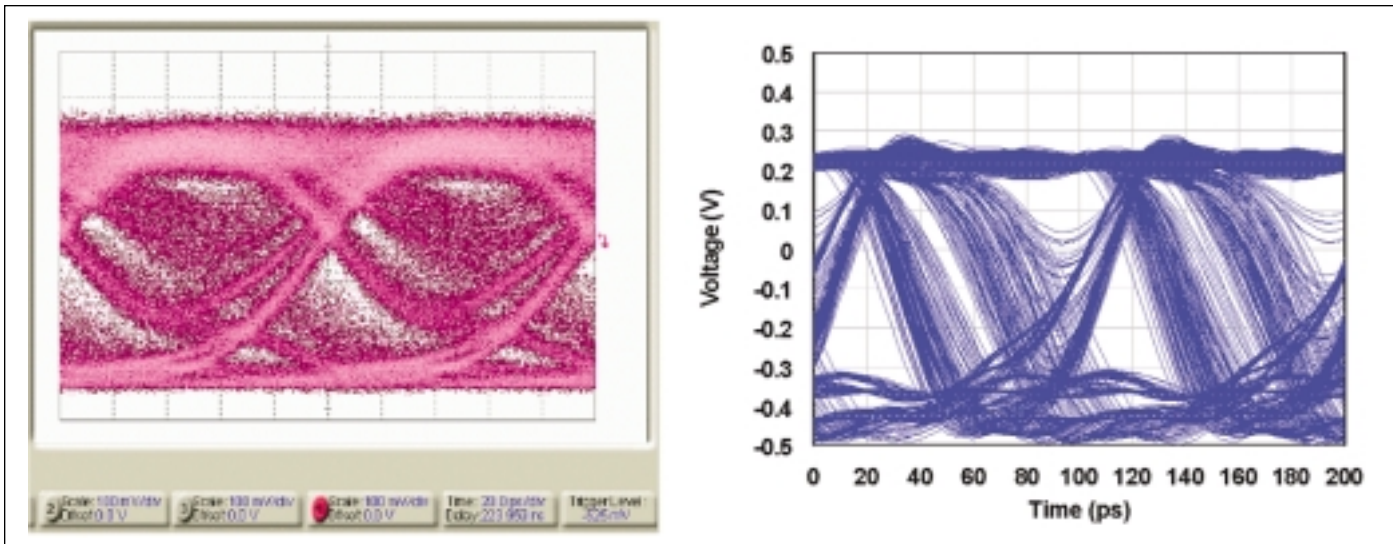
Triquint HDI specific rules file that runs in Microwave Office 2002's interactive verification tool. The complete system enables the design engineer to quickly create a layout that has verified layout cells, correct interconnects and an overall design that can be verified for geometry errors.

By looking at the chip design cycle as a whole, there was a great opportunity to reduce time on the back end by automatically creating the documentation necessary for the foundry hand-off. The Microwave Office 2002 software's component object model (COM) interface enables direct access to the project database from external tools, such as Microsoft Excel and Microsoft Word. The Fast Chips process can automatically generate most of the required documentation, such as parts list, capacitance area, resistor area, active device area, die size and probe card information, by querying the Microwave

Office 2002 database and writing out documentation files. The documentation remains synchronized to the central database, and any change in the design can be instantaneously updated in the project documentation. The COM application programming interface (API) also supports automatic generation of the DC schematic (in netlist format), required for the LVS geometry checks at manufacturing sign-off for the chip. The Fast Chips PDK greatly reduces cycle time and, most importantly, reduces errors by keeping track of all design representations in a single location enabling MMIC designers to concentrate on creating innovative high-performance designs.

Conclusion

Fast Chips is a timely collaboration that is bringing about process and library improvements that are reduc-



▲ Figure 11. TGA4805 simulation versus measured data EYE diagram for optical input power exceeding overload condition.

ing design time and improving the performance of high-speed ICs. The efforts are being commercialized in the form of advanced PDKs that are available from TriQuint and operate in the Microwave Office 2002 design environment. Foundry libraries are available to TriQuint's foundry customers for the 0.15 um and 0.25 um pHEMT processes. The Fast Chips efforts are focused on commercializing the new HDI pHEMT processes from TriQuint and availability of these libraries is scheduled for July 2002. For more information on TriQuint foundry services, contact TriQuint Semiconductor at 503-615-9000. Foundry libraries are provided at no additional cost to Microwave Office 2002 product users with foundry contracts and current maintenance agreements. Microwave Office 2002 software is available from Applied Wave Research, Inc. For more information, contact AWR at 310-726-3000 or go to www.mwoffice.com. ■

Author information

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William Reinisch is the executive director of technology for Multilink Technology Corporation, Somerset, NJ. He has been involved in many different aspects of semiconductor technology, including extensive experience with both GaAs- and Si-based technologies and foundry operations. He has a bachelor of science degree in microelectronic engineering from Rochester Institute of Technology and an MBA from Fordham University.

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